

FEATURES

- ◆ Plastic package has Underwriters Laboratory Flammability Classification 94V-0
- ◆ For surface mounted applications
- ◆ Low profile package
- ◆ Built-in strain relief, ideal for automated placement
- ◆ Glass passivated chip junction
- ◆ High temperature soldering: 250°C/10 seconds at terminals

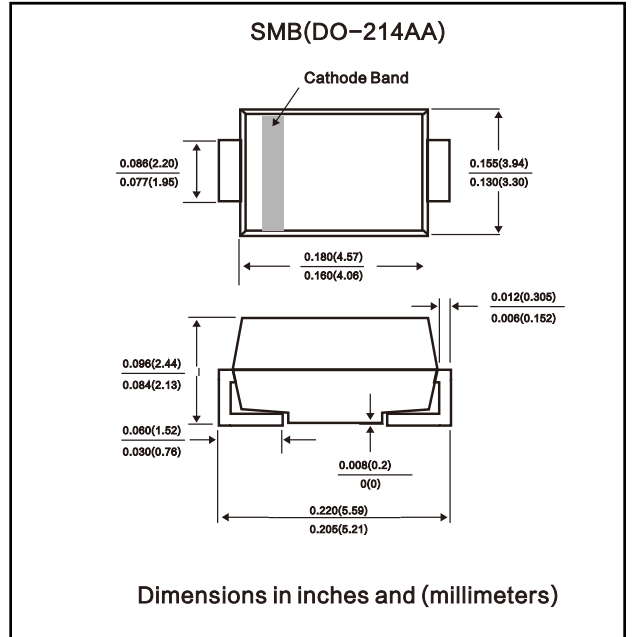
MECHANICAL DATA

Case: JEDEC DO-214AA molded plastic over passivated chip

Terminals: Solder plated, solderable per MIL-STD-750, Method 2026

Polarity: Color band denotes cathode end

Weight: 0.002 ounce, 0.064 gram



MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	S2A	S2B	S2D	S2G	S2J	S2K	S2M	Unit
Peak Repetitive Reverse Voltage	V_{RRM}	50	100	200	400	600	800	1000	V
Working Peak Reverse Voltage	V_{RWM}								
DC Blocking Voltage	V_R								
RMS Reverse Voltage	$V_{R(RMS)}$	35	70	140	280	420	560	700	V
Average Rectified Output Current @ $T_L = 110^\circ\text{C}$	I_O	2.0							A
Non-Repetitive Peak Forward Surge Current 8.3ms Single half sine-wave superimposed on rated load (JEDEC Method)	I_{FSM}	60							A
Forward Voltage @ $I_F = 2.0\text{A}$	V_{FM}	1.10							V
Peak Reverse Current @ $T_A = 25^\circ\text{C}$	I_{RM}	5.0							μA
At Rated DC Blocking Voltage @ $T_A = 125^\circ\text{C}$		200							
Reverse Recovery Time (Note 1)	t_{rr}	2.5							μs
Typical Junction Capacitance (Note 2)	C_j	30							pF
Typical Thermal Resistance (Note 3)	$R_{\theta JL}$	16							K/W
Operating and Storage Temperature Range	T_j, T_{STG}	-55 to +150							$^\circ\text{C}$

Note: 1. Measured with $I_F = 0.5\text{A}$, $I_R = 1.0\text{A}$, $I_{rr} = 0.25\text{A}$,
 2. Measured at 1.0 MHz and applied reverse voltage of 4.0 V DC.
 3. Mounted on P.C. Board with 8.0mm² land area.

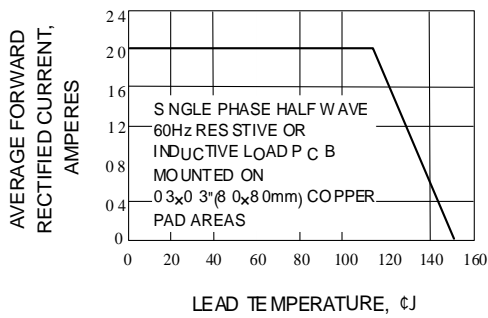


Fig. 1-FORWARD CURRENT DERATING CURVE

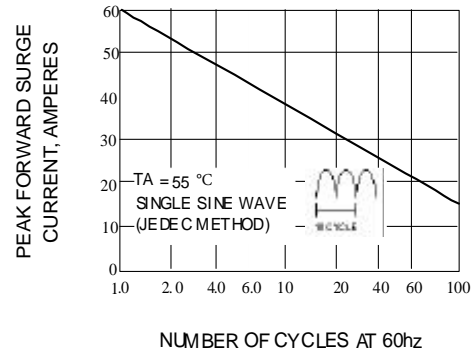


Fig. 2-MAXIMUM NON-REPETITIVE PEAK FORWARD SURGE CURRENT

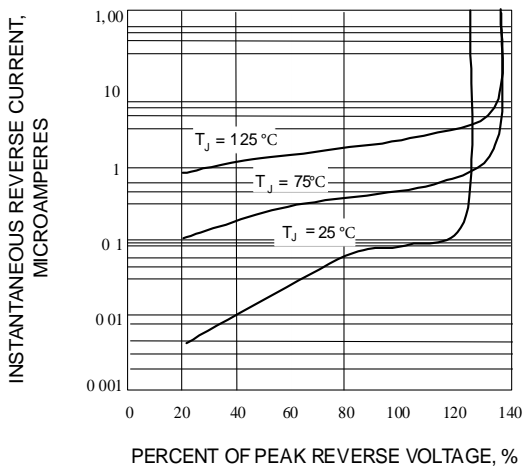


Fig. 3-TYPICAL REVERSE CHARACTERISTICS

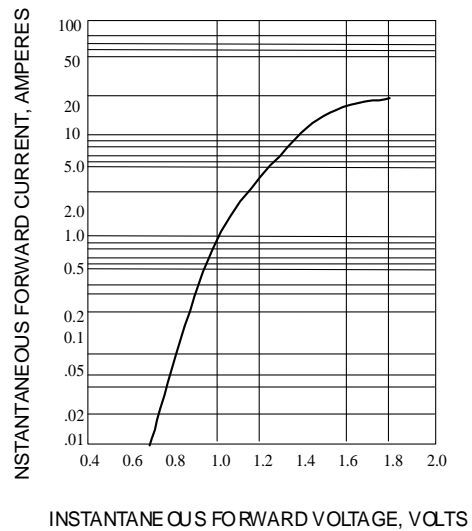


Fig. 4-TYPICAL INSTANTANEOUS FORWARD CHARACTERISTICS

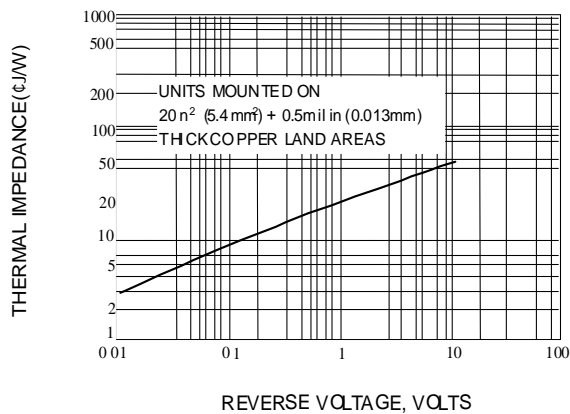


Fig. 5 TRANSIENT THERMAL IMPEDANCE

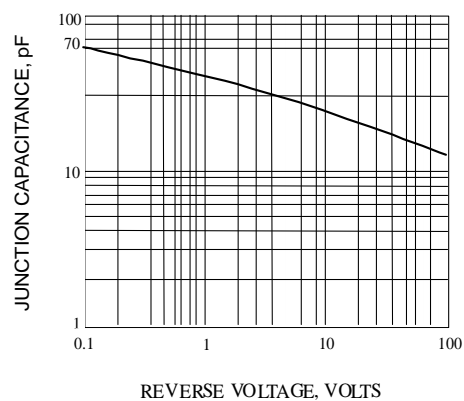


Fig. 6 TYPICAL JUNCTION CAPACITANCE