

1-Line, Bi-directional, Transient Voltage Suppressor

Features

- Stand-off voltage: $\pm 7V$ Max.
- Transient protection for each line according to
IEC61000-4-2(ESD): $\pm 30kV$ (contact)
IEC61000-4-4 (EFT): 40A (5/50ns)
IEC61000-4-5(surge): 6A (8/20 μs)
- Ultra-low capacitance: $C_J = 10pF$ typ.
- Low leakage current:
- Low clamping voltage: $V_{CL} = 12.0V$ typ. @ $I_{PP} = 16A$ (TLP)
- Solid-state silicon technology

Applications

- Cellular handsets
- USB V_{BUS} and CC Line Protection
- Microphone Line Protection
- GPIO Protection

Descriptions

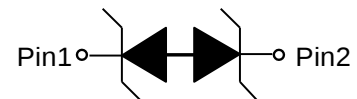
PESDU0711P0A is a bi-directional TVS (Transient Voltage Suppressor). It has been specifically designed to protect sensitive electronic components which are connected to low speed data lines and control lines from over-stress caused by ESD (Electrostatic Discharge), EFT (Electrical Fast Transients) and Lightning.

PESDU0711P0A may be used to provide ESD protection up to $\pm 30KV$ (contact discharge) according to IEC61000-4-2, and withstand peak pulse current up to 6A (8/20 μs) according to IEC61000-4-5.

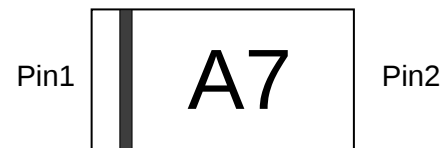
PESDU0711P0A is available in DFN0603-2 package. Standard products are Pb-free and Halogen-free.



DFN0603-2 (Bottom View)



Pin configuration



A7= Device code

Marking (Top View)

Order information

Device	Package	Shipping
PESDU0711P0A	DFN0603-2	10000/Tape & Reel

Absolute maximum ratings

Parameter	Symbol	Rating	Unit
Peak pulse power ($t_p = 8/20\mu s$)	P_{pk}	84	W
Peak pulse current ($t_p = 8/20\mu s$)	I_{PP}	6	A
ESD according to IEC61000-4-2 air discharge	V_{ESD}	± 30	kV
ESD according to IEC61000-4-2 contact discharge		± 30	
Junction temperature	T_J	125	$^{\circ}C$
Operating temperature	T_{OP}	-40~85	$^{\circ}C$
Lead temperature	T_L	260	$^{\circ}C$
Storage temperature	T_{STG}	-55~150	$^{\circ}C$

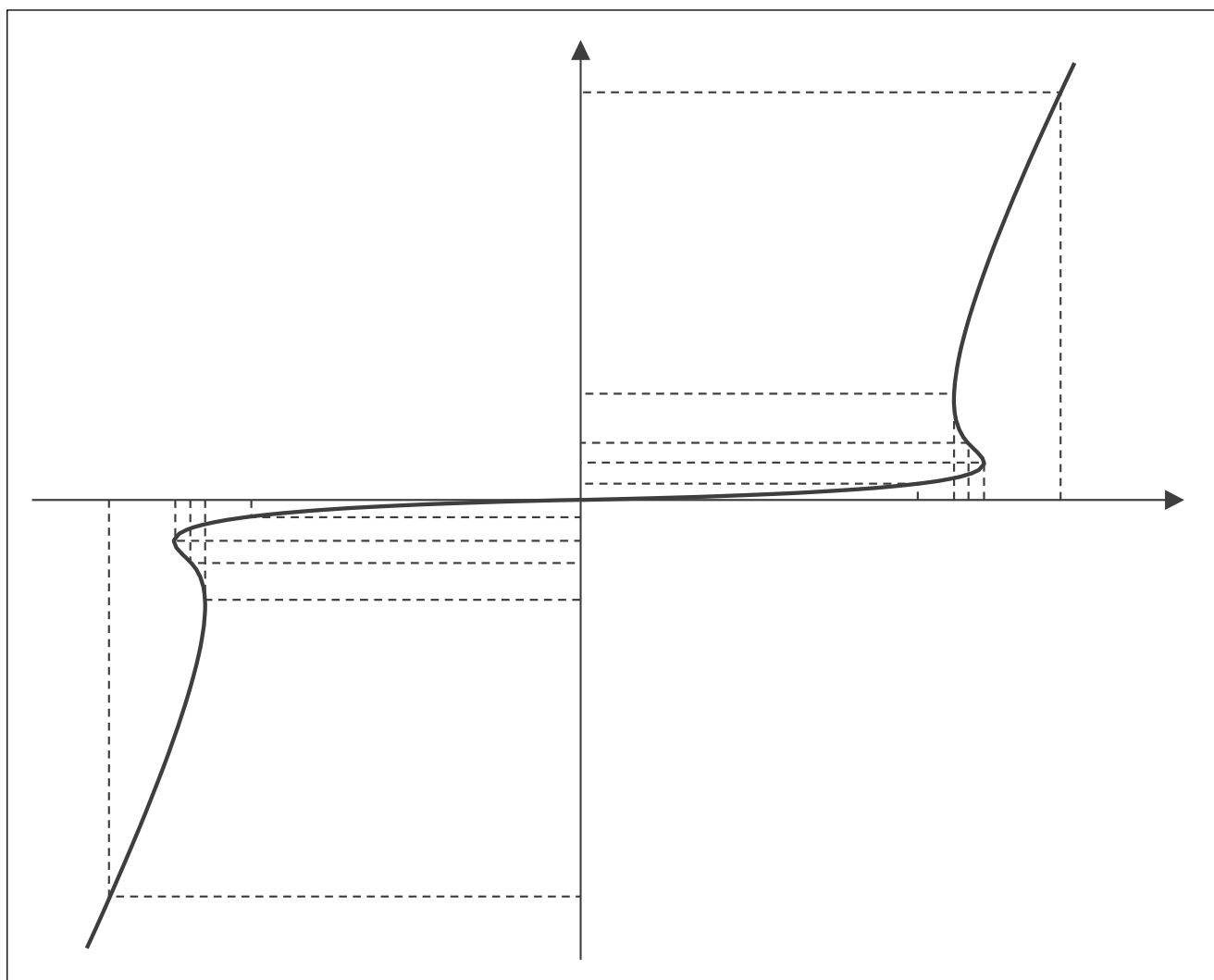
Electrical characteristics ($T_A = 25^{\circ}C$, unless otherwise noted)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reverse maximum working voltage	V_{RWM}				± 7	V
Reverse leakage current	I_R	$V_{RWM} = 7V$			100	nA
Reverse breakdown voltage	V_{BR}	$I_{BR} = 1mA$	7.2		10.5	V
Reverse holding voltage	V_{HOLD}	$I_{HOLD} = 50mA$	7.2		10.5	V
Clamping voltage ¹⁾	V_{CL}	$I_{PP} = 16A, t_p = 100ns$		12.0		V
Dynamic resistance ¹⁾	R_{DYN}			0.28		Ω
Clamping voltage ²⁾	V_{CL}	$V_{ESD} = 8kV$		12.0		V
Clamping voltage ³⁾	V_{CL}	$I_{PP} = 1A, t_p = 8/20\mu s$		9	11	V
		$I_{PP} = 6A, t_p = 8/20\mu s$		12	14	V
Junction capacitance	C_J	$V_R = 0V, f = 1MHz$		10	13	pF
	C_J	$V_R = 2.5V, f = 1MHz$		8	11	pF

Notes:

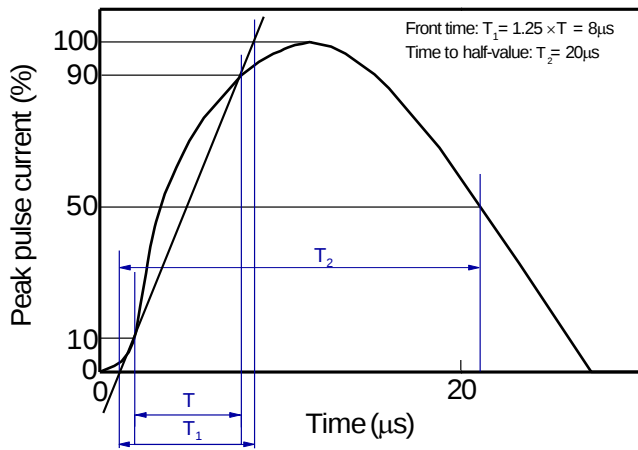
- 1) TLP parameter: $Z_0 = 50\Omega$, $t_p = 100ns$, $t_r = 2ns$, averaging window from 60ns to 80ns. R_{DYN} is calculated from 4A to 16A.
- 2) Contact discharge mode, according to IEC61000-4-2.
- 3) Non-repetitive current pulse, according to IEC61000-4-5.

Electrical characteristics ($T_A=25\text{ }^{\circ}\text{C}$, unless otherwise noted)

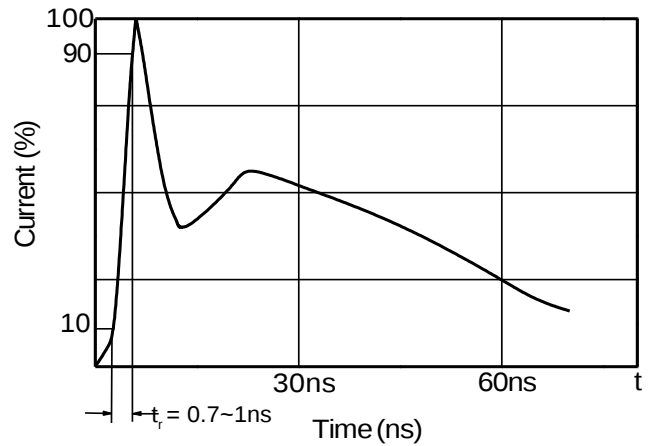


Definitions of electrical characteristics

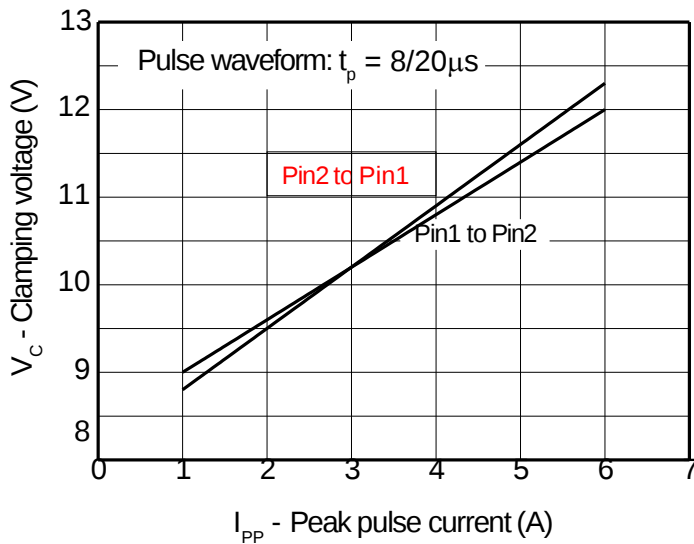
Typical characteristics (TA = 25 °C, unless otherwise noted)



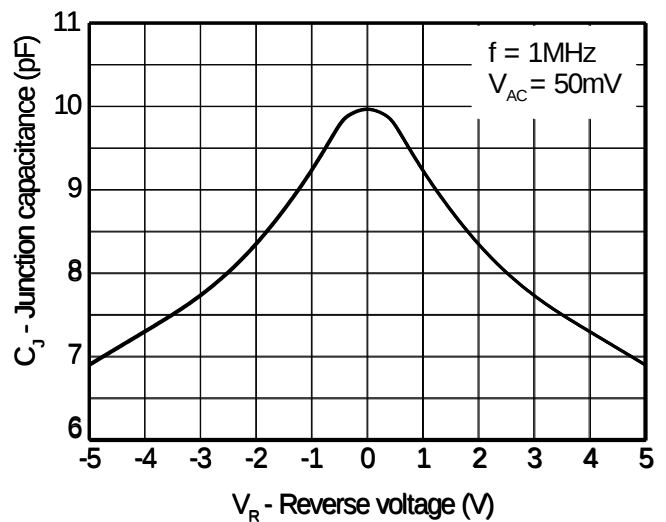
8/20μs waveform per IEC61000-4-5



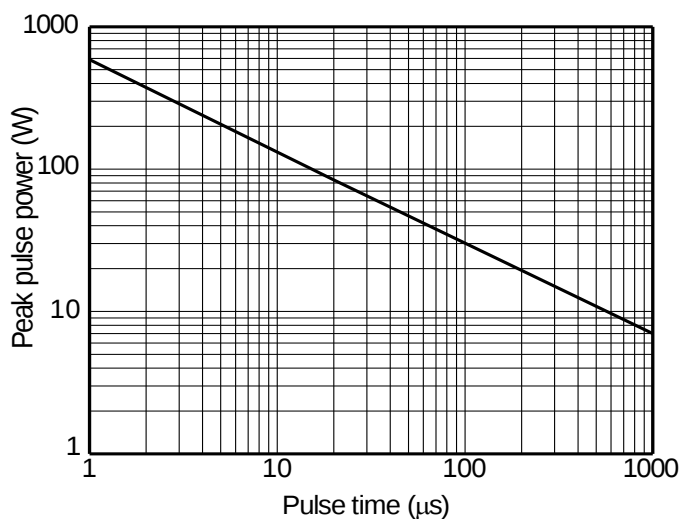
Contact discharge current waveform per IEC61000-4-2



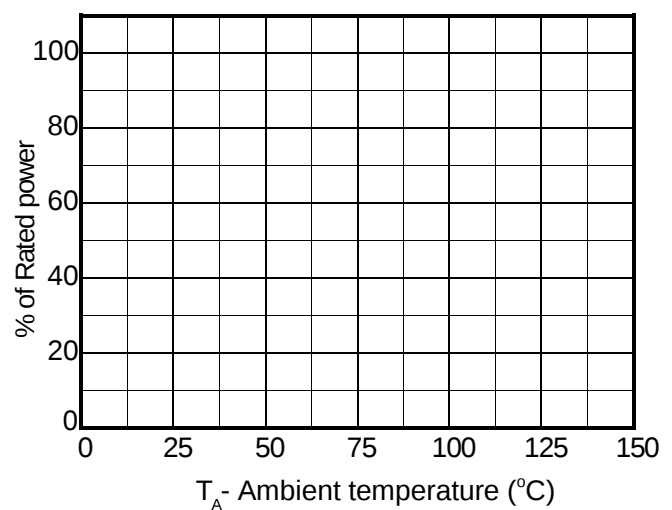
Clamping voltage vs. Peak pulse current



Capacitance vs. Reverse voltage

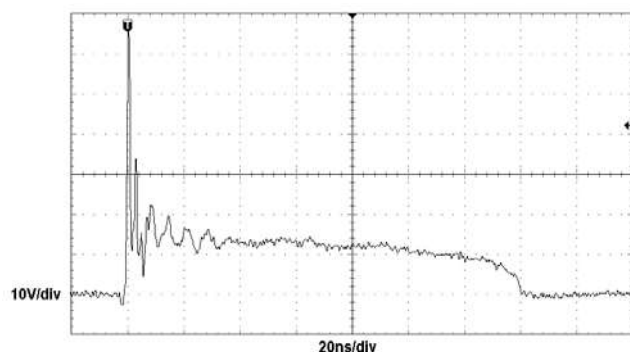


Non-repetitive peak pulse power vs. Pulse time

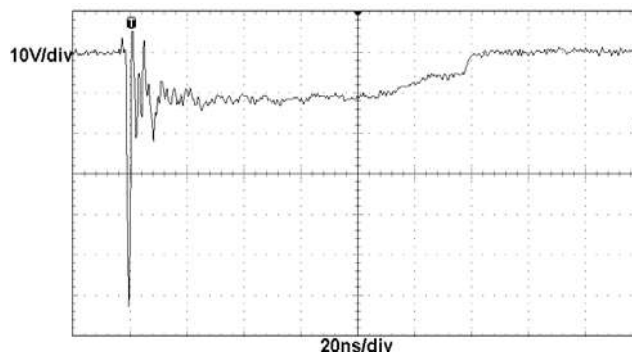


Power derating vs. Ambient temperature

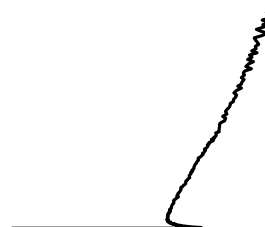
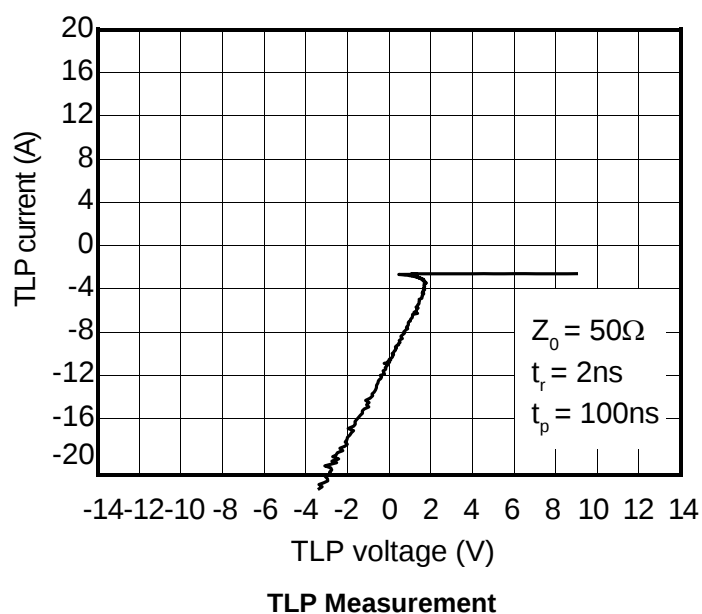
Typical characteristics (TA = 25 °C, unless otherwise noted)



ESD clamping
(+8kV contact discharge per IEC61000-4-2)

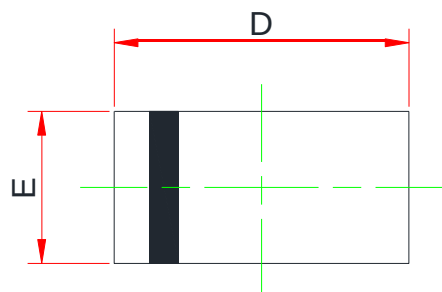


ESD clamping
(-8kV contact discharge per IEC61000-4-2)

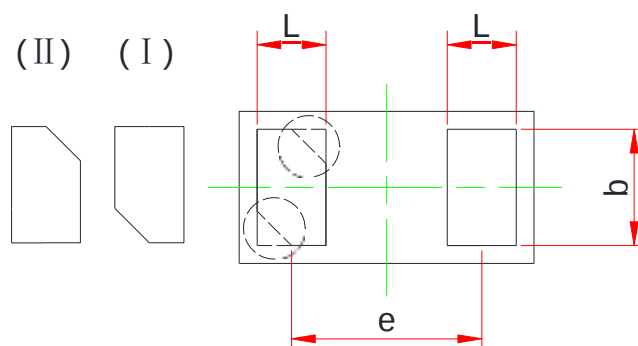


PACKAGE OUTLINE DIMENSIONS

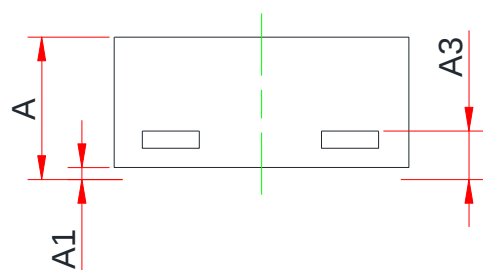
DFN0603-2



Top View

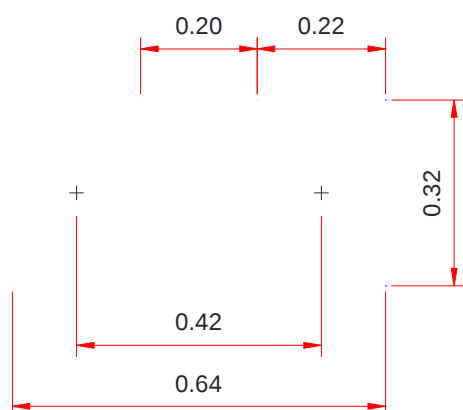


Bottom View



Side View

Recommend land pattern (Unit: mm)



Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.230	-	0.340
A1	0.000	-	0.050
A3	0.102 REF.		
D	0.550	0.600	0.670
E	0.250	0.300	0.370
b	0.215	-	0.295
e	0.400 BSC		
L	0.115	-	0.195

Notes:

This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met.